Adding a Manual Reset to Intersil CPU Supervisors

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Introduction

The Intersil CPU Supervisors provides a number of important system monitoring and reset functions that help insure high system reliability (See Application Note AN108.) However, there are times when it is desired to also include a manual reset switch. This application note explores several different approaches.

Force the Reset

The first, simplest, solution is to add a “debounced switch to the $\overline{\text{RESET}}$ signal (See Figure 1.) In this circuit, the open drain $\overline{\text{RESET}}$ output of the Supervisory EEPROM is pulled HIGH to give the normal, inactive reset signal to the microcontroller. The manual reset switch pulls down the RESET signal, with the capacitor providing some debounce.

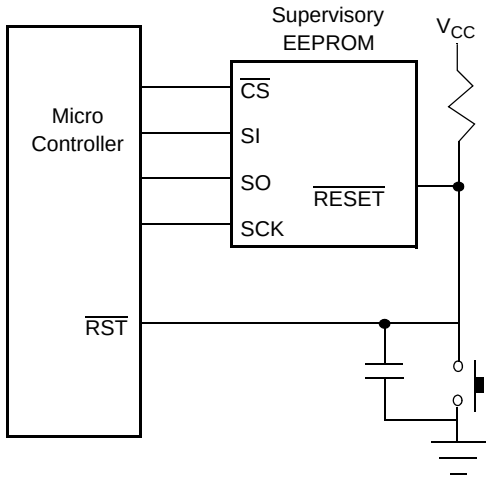

Figure 1. Reset Switch (Active LOW Reset)

The main disadvantage to this circuit is that the length of the pulse is indeterminate, which might result in some problems with some controllers. A second problem with this solution is that it doesn’t work well with an active HIGH reset signal. In this case (See Figure 2.), the RESET output is pulled up, but is normally LOW. Adding a switch to pull RESET HIGH results in contention in the output driver. It will work, but can put strain on the output buffer.

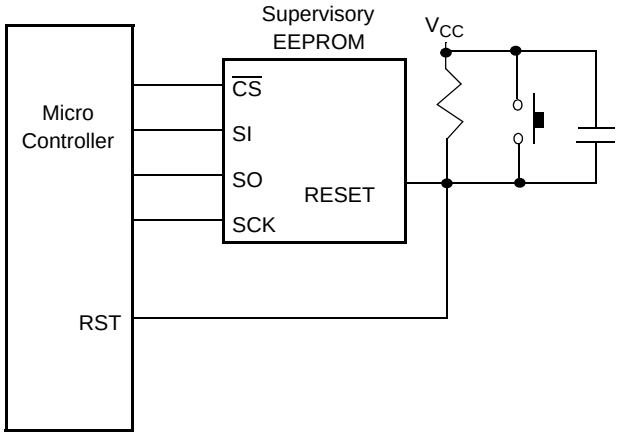

Figure 2. Reset Switch (Active HIGH Reset)

Use Low Voltage Reset

A mechanism that works for both active HIGH and active LOW reset makes use of the Intersil CPU supervisor low voltage sense circuit. In this case, a switch and three diodes are added to the Vcc line of the supervisor (See Figure 3.) Opening the switch drops the power to the CPU supervisor only, from above 4.55V to below 4.25 volts. As power to the Vcc line drops below the trip point, the reset pin goes active, resetting the system. The supervisor then provides a clean reset signal and doesn’t release the reset signal for 250ms (nominal) after the Vcc supply returns. The reset output is pulled up to 5V providing either an active HIGH or active LOW reset.

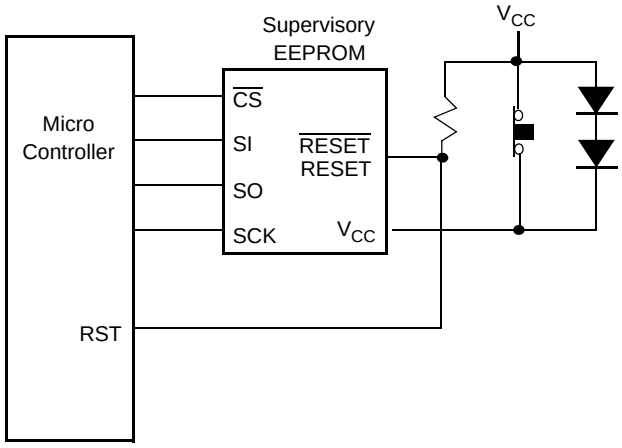

Figure 3. Using the Low Voltage Reset

Use Watchdog Timer

The built in Watchdog timer can also be used to create a debounced manual switch. With the Supervisory EEPROM watchdog timer turned on, a switch can be added into the chip select line (See Figure 4.) to control the reset signal reaching the $\overline{CS}$ pin. Normally this signal restarts the watchdog timer, preventing a reset condition. When the reset switch is pressed, however, the chip select signal from the microcontroller is disconnected from the Supervisor. This prohibits the timer from being restarted and the watchdog timer expires within a preset time period. When the watchdog period is set to 200 ms, the reset operation responds in a reasonable amount of time. Also, since the watchdog timer reset action occurs only periodically, it effectively acts to debounce the reset switch. This circuit is limited by the need to use the 200ms setting, but the presence of the watchdog timer can provide a manual reset input for systems that use a second watchdog timer in another part of the circuit for system management.

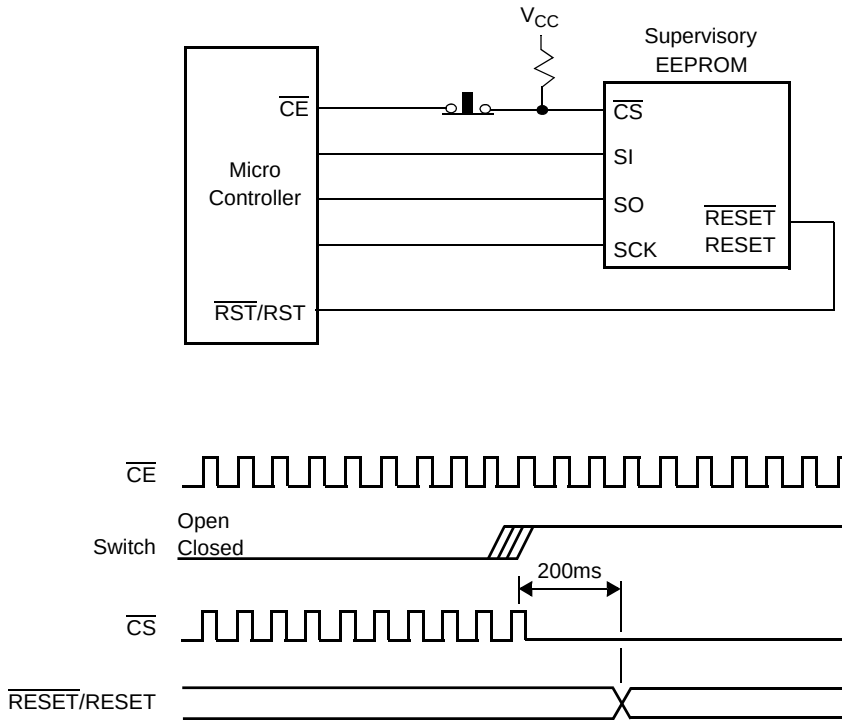

Figure 4. Using the Watchdog Timer for Debounced Manual Reset